A 3.4V, 1 Watt Cellular DAMPS GaAs MESFET Power Amplifier with 50% Efficiency

Stewart S. Taylor
TriQuint Semiconductor, 2300 NE Brookwood Parkway
Hillsboro, Oregon 97124 USA, (503) 615-9372, staylor@tqs.com

ABSTRACT

A 3.4V, 1 Watt cellular DAMPS power amplifier with 50% efficiency has been implemented and tested. The single-supply PA incorporates biasing, PMOS interface, and negative supply voltage generation on-chip, and is assembled in a TSSOP20 package with a downset paddle. The circuit achieves 30dB of power gain, a 12dB input return loss, and is implemented in a 20GHz ion-implanted GaAs MESFET manufacturing process.

Figure 1 is a block diagram of the power amplifier. It consists of a two gain stages, bias circuitry, a negative supply generator, and PMOS interface circuit/negative supply sense. The simplified core PA is shown in Figure 2. The input matching network consists of L1 and C1 while the interstage matching network consists of L2, C2, and L6. R1 and C6 improve the amplifier stability. The output matching network is composed of L4 and C3. L3 is an RFC and C4 is a DC block. The output transistor periphery is 19mm.

Figure 3 shows a simplified current mirror bias circuit that establishes the drain current of dummy transistor Q1 through the use of negative feedback with amplifier A1. I_2, the bias current of the transistor in one of the RF amplifiers, scales with I_1 according to

$$I_2 \cong I_1 \frac{W_2}{W_1} \cong \frac{V_1}{R_1} \frac{W_2}{W_1}$$

Two of these circuits form Vbias1 and Vbias2 shown in Figure 2. An important feature of the bias amplifier in the current mirror is to operate class AB when sinking current. A simplified circuit diagram of this output stage is shown in Figure 3. Q3 establishes the nominal bias current in source follower Q1 and pull down transistor Q2. When Vout goes sufficiently positive, the gate voltage of Q2 is increased by Q3 and Q4, which go positive. This allows Q2 to accommodate up to 8mA of leakage current from the gate of the FET if necessary while standing less than 0.5mA. There is also a series resonant RF trap connected (not shown) from the output of the bias amplifier to ground to suppress the RF signal. This is necessary to avoid overload and a corresponding bias point shift under conditions of large RF drive.

The bias current in the first stage is chosen to be relatively low (10mA). It is found experimentally and with computer simulation that operating the first stage in compression creates an AM/PM curve that partially compensates for that of the output stage. This allows the amplifier to be driven more into compression while meeting adjacent channel power ratio (AdjCPR) and alternate channel power ratio (AltCPR), improving efficiency. If the bias current of the first stage is too low, the AltCPR is too large. If the bias current is too high, the AdjCPR is too large. The low bias current in the input stage allows the output stage to be biased at a lower current, improving efficiency.

Figure 4 is a simplified schematic diagram of the PMOS interface circuit which includes a negative supply voltage sense. This latter feature is essential to protect the amplifier in case the negative

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

supply is not present for any reason, including excessive gate leakage in the output transistor. It also delays the turn-on of the PMOS switch until the negative supply is sufficiently large to reduce large DC currents in the amplifier FETs. PAon passes through a noninverting gate whose threshold is set to 1.5V. The output of this buffer drives a NAND gate whose other input is driven by the cascade of two inverters, the first of which has its input connected to the negative supply. The threshold of this negative supply sense is set by the pinchoff voltage of a FET and several diodes to be approximately -2.5V.

Figure 5 is a simplified schematic diagram of the negative supply generator, which is a voltage doubler. This was required for 2.7V operation with MESFETs with -2.7V worst-case pinchoff voltage since the bias circuitry requires voltage headroom for the transistors to operate in saturation. The voltage doubler consists of two driver circuits, coupling and filter capacitors C1-C3, and rectifying diode-connected EFET transistors Q1-Q3. The diode-connected EFETs rectify with less voltage loss than Schottky diodes, producing a more negative output voltage.

Figure 6 shows simplified circuits for the relaxation oscillator and driver for the voltage doubler. The oscillator frequency is nominally 15MHz, with maximum spurious output levels of -80dBc. The driver circuit is an AC coupled emulation of a standard super-buffered bootstrapped NMOS circuit. The gates of DFETs Q3 and Q5 can be taken below ground to shut them off while the gate of EFET Q6 can be driven above Vdd to make its Vds very small. This results in an efficient circuit that swings within 0.1V of ground and Vdd.

Table 1 is a summary of the performance of the power amplifier, which is assembled in a TSSOP20 package with a down-set paddle that enhances the thermal and electrical performance. Figure 7 shows the adjacent and alternate channel power ratios for 30dBm output power. Figure 8 is a die photo.

The circuit is implemented in a low-power, ion-implanted, GaAs MESFET manufacturing process depicted in Figure 9. This process has enhancement and depletion transistors, 50 ohm per square thin-film NiCr resistors, 1200pF/mm^2 MIM capacitors, and three-level, low-dielectric gold interconnect. The upper two interconnect layers are 2um and 4um thick, respectively, and can be stacked to make transformers and inductors with Q's of 20. Three FETs are available, two depletion devices and one enhancement device, with pinch-off voltages of -2.2V, -0.6V, and 0.15V, respectively. f_t and f_{max} are 20GHz and 50GHz, respectively. The -2.2V device achieves 400mA/mm of peak drain current.

ACKNOWLEDGMENTS

The author would like to acknowledge the contribitions of Rich Schwab, Ed Knapp, Dennis Kruger, Sam Hammond, Randy Cooper, Rich McClure, John Liebenrood, Soufi Azghandi, Keith Jones, Carl Stuebing, Andy Ross, Karen Wallace, and Ken Mays.

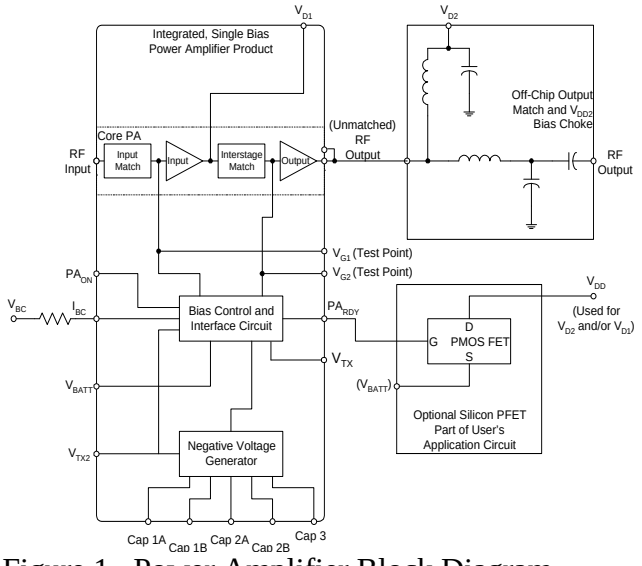


Figure 1. Power Amplifier Block Diagram

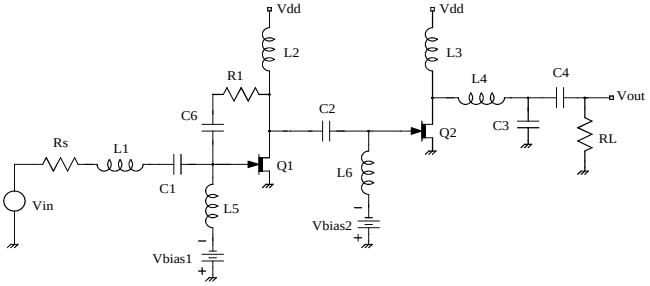
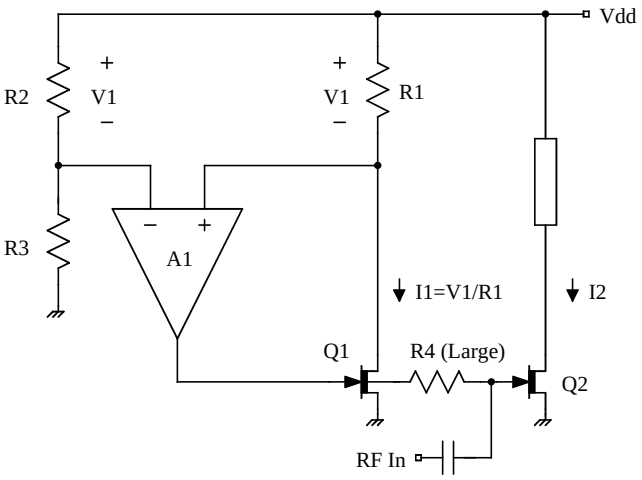


Figure 2. Simplified Power Amplifier



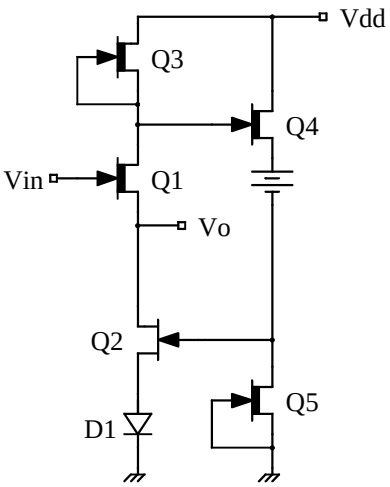


Figure 3. Simplified Biasing and Output Stage

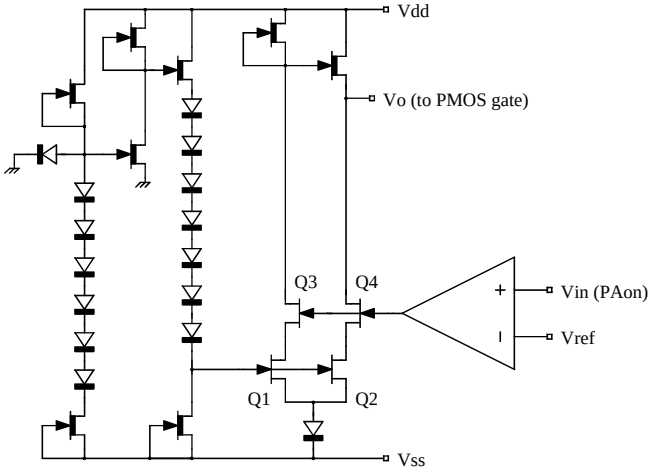


Figure 4. Interface Circuit & Neg. Supply Sense

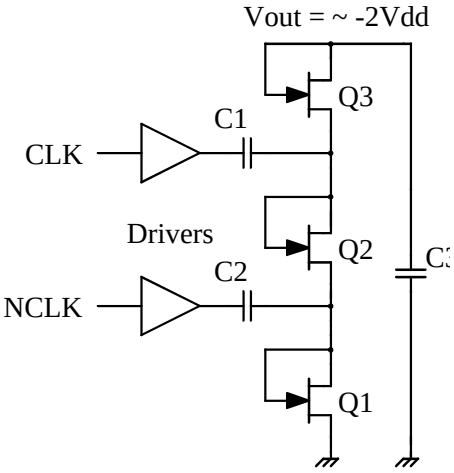
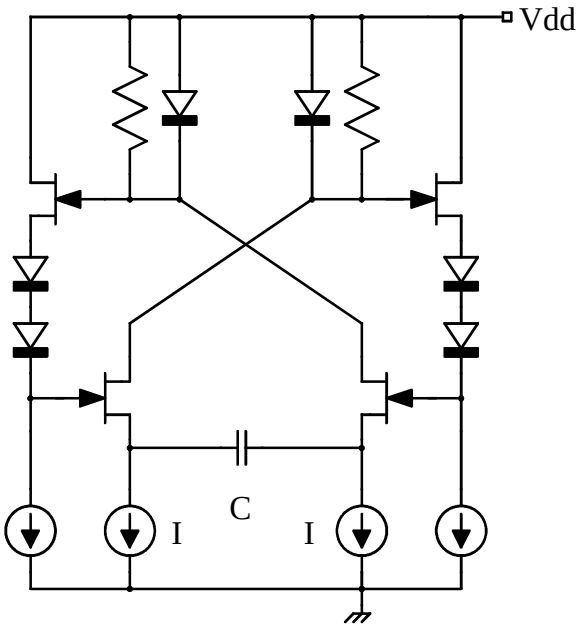


Figure 5. Simplified Voltage Doubler



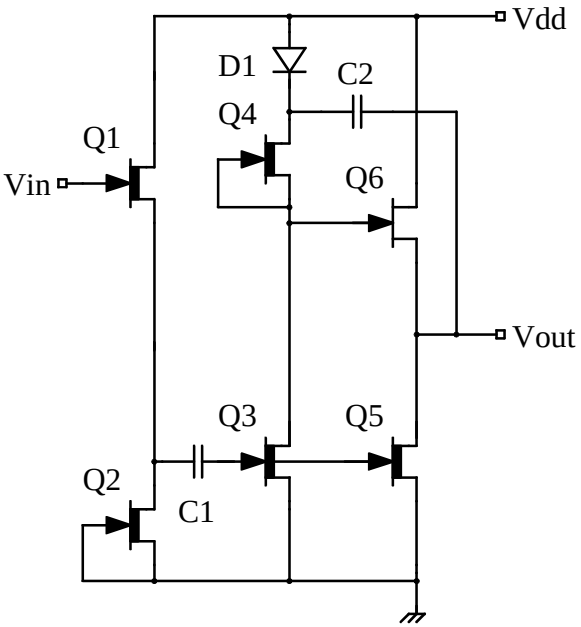


Figure 6. Simplified Oscillator and Driver

Po	Vbatt	η @ Po	S11	S21	AdjCPR	AltCPR	Load	Rugg. & Stability
30dBm	3.4V	45%	-12dB @ 10dBm	30dB @ 10dBm	-30dBc	-50dBc	2:1 VSWR, All ∠s	10:1 VSWR in-Band
31dBm	3.4V	50%			-27dBc	-46dBc	50 ohms	10:1 VSWR in-Band

Table 1. Performance Summary

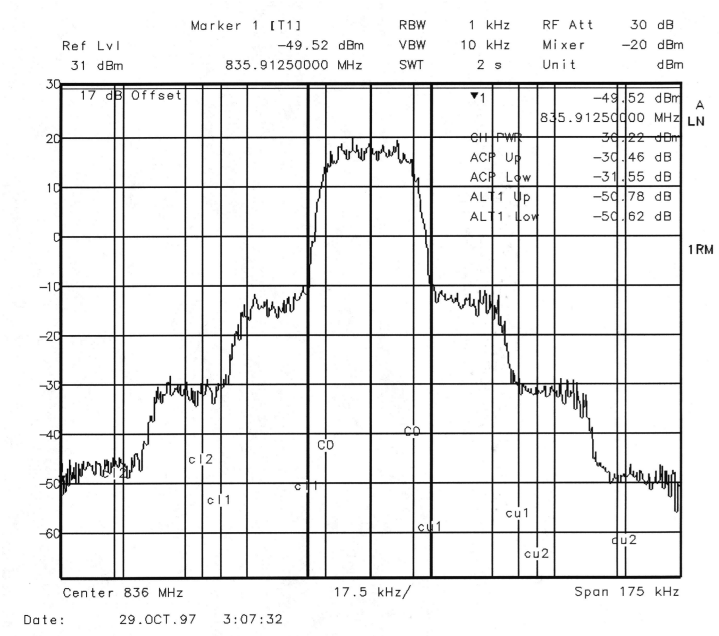


Figure 7. AdjCPR and AltCPR at 30dBm

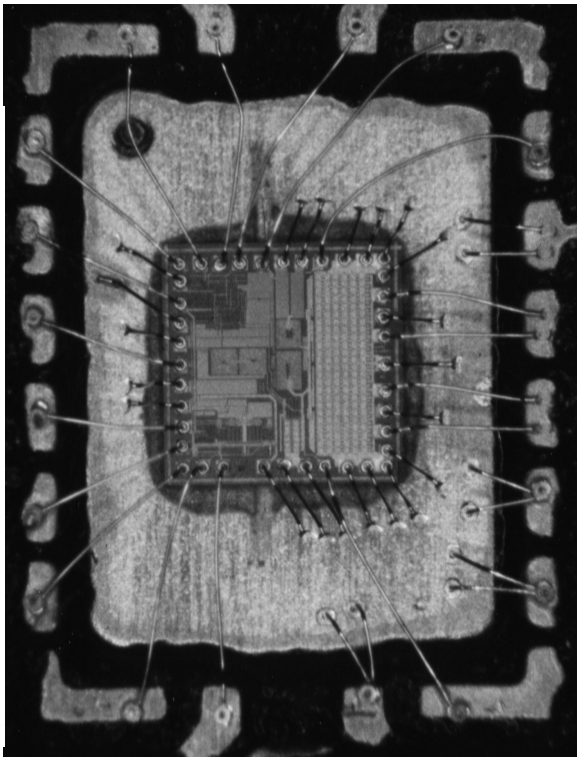


Figure 8. Die/Package Cavity Photo

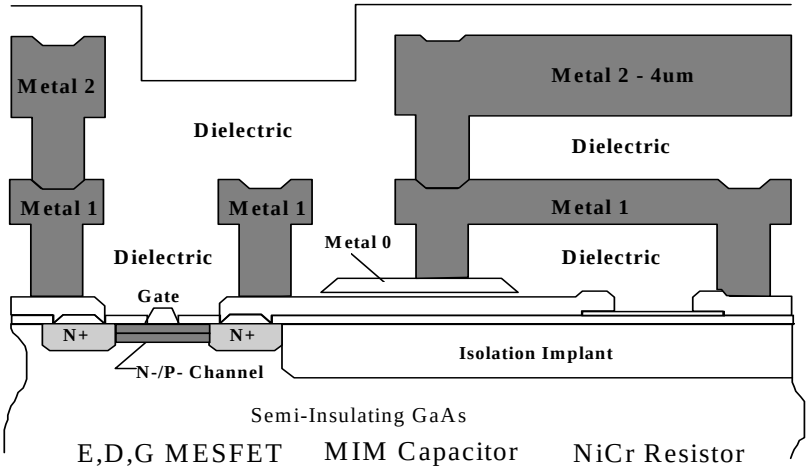


Figure 9. GaAs MESFET Process

- RF Transceiver Process
- Vt = 0.15V EFET
- Vt = -0.6V DFET
- Vt = -2.2V GFET
- Three Layer Metal
- Low ε BCB Dielectric
- f_{max} = 50GHz
- C/A = 1200pF/mm^2
- Q = 20 @ 2GHz